



CFW 2122

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

**SUPPLEMENTAL INFORMATION  
DISCLOSURE STATEMENT**

Docket Number:  
**02885/87**

Application Number  
**10/501,903**

Filing Date  
**March 1, 2005**

Examiner  
**To be assigned**

Art Unit  
**2122**

Invention Title  
**METHOD OF COMPILATION**

Inventor  
**Martin VORBACH et al.**

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on

Date: 7 Nov 2005

Signature: [Signature]  
**Michelle Carniaux**

*Reg No 4011*

SIR:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable. It is believed that no fees other than those indicated below are due, but authorization is hereby given to charge any additional fees due, or to credit any overpayment, to **Kenyon & Kenyon LLP, deposit account 11-0600**.

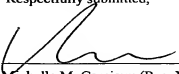
☒ 1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. § 1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d) before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

☒ 2. English-language Abstract of the non-English language reference is attached hereto.

- ☒ 3. Since this application was filed after June 30, 2003, copies of U.S. references are not included.

Respectfully submitted,

Dated: 7 November

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.C./

**SUPPLEMENTAL  
INFORMATION DISCLOSURE  
STATEMENT BY APPLICANTS  
PTO-1449**

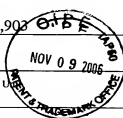
Attorney Docket No.  
2885/87

Serial No.  
10/501,903

Applicant(s)  
VORBACH et al.

Filing Date  
March 1, 2005

Group Art U  
2122



**U.S. PATENT DOCUMENTS\***

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,489,857	February 6, 1986	Agrawal et al.			
	4,720,780	January 19, 1988	Dolecek			
	5,600,845	February 4, 1997	Gilson			
	6,697,979	February 24, 2004	Vorbach et al.			
	6,728,871	April 27, 2004	Vorbach et al.			
	2002/0045952	April 18, 2002	Blemel			
	2004/0168099	August 26, 2004	Vorbach et al.			
	2001/0010074	July 26, 2001	Nishihara et al.			

\*In accordance with 37 C.F.R. (a)(2)(ii), copies of each of the cited U.S. patents and U.S. patent applications publications are not being provided.

**FOREIGN PATENT DOCUMENTS<sup>1</sup>**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 208 457	January 14, 1987	EPO				
	0 735 685	October 2, 1996	EPO				
	0 726 532	August 14, 1996	EPO				
	100 28 397	December 20, 2001	Germany			Abstract	
	100 36 627	February 14, 2002	Germany			Abstract	
	101 29 237	April 18, 2002	Germany			Abstract	
	102 04 044	August 14, 2003	Germany			Abstract	
	8-44581	February 16, 1996	Japan			Abstract+	
	7-154242	June 16, 1995	Japan			Abstract+	
	58-58672	April 7, 1983	Japan			Abstract+	
	2-226423	September 10, 1990	Japan			Abstract+	
	5-276007	October 22, 1993	Japan			Abstract+	
	8-250685	September 27, 1996	Japan			Abstract+	
	2-130023	May 18, 1990	Japan			Abstract+	
	WO 99/12111	March 11, 1999	WIPO				
	WO 01/55917	August 2, 2001	WIPO				

+ = English Abstract plus patent family equivalents

**OTHER DOCUMENTS**

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Athanas, "A Functional Reconfigurable Architecture and Compiler for Adoptive Computing," IEEE (1993), pages 49-55.
	Baumgart, V., et al., PACT XPP "A Self-reconfigurable Data Processing Architecture," PACT Info. GMBH, Munchen Germany, 2001, 7 pages.
	Beck et al., "From control flow to dataflow," Department of Computer Science, Cornell Univ., Ithaca, NY (October 1989), pp. 1-25.

<b>SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. 2885/87	Serial No. 10/501,903
	Applicant(s) <b>VORBACH et al.</b>	
	Filing Date March 1, 2005	Group Art Unit 2122

	Becker, J. et al., "Parallelization in Co-compilation for Configurable Accelerators - a Host/accelerator Partitioning Compilation Method," proceedings of Asia and South Pacific Design Automation Conference, Yokohama, Japan, February 10-13, 1998, 11 pages.
	<b>**Cardoso, J.M.P., "Compilation of Java™ Algorithms onto Reconfigurable Computing Systems with Exploitation of Operation-Level Parallelism," Ph.D. Thesis, Universidade Tecnica de Lisboa (UTL), Lisbon, Portugal October 2000 (Table of Contents and English Abstract only).</b>
	<b>**Hammes, Jeff et al., "Cameron: High Level Language Compilation for Reconfigurable Systems," Department of Computer Science, Colorado State University, Conference on Parallel Architectures and Compilation Techniques, October 12-16, 1999, 9 pages.</b>
	<b>**Hauser, J.R. et al., "Garp: A MIPS Processor with a Reconfigurable Coprocessor", University of California, Berkeley, IEEE, 1997, pages 24-33.</b>
	Jantsch, Axel et al., "A Case Study on Hardware/software Partitioning," Royal Institute of Technology, Kista, Sweden, April 10, 1994 IEEE, pp. 111-118.
	<b>**Myers, G. "Advances in Computer Architecture," Wiley-Interscience Publication, 2nd ed., John Wiley &amp; Sons, Inc., 1978, pp. 463-494.</b>
	<b>**Mirsky, E., et al, "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources," Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, 1996, pp. 157-166.</b>
	Shirazi, et al., "Quantitative analysis of floating point arithmetic on FPGA based custom computing machines," IEEE Symposium on FPGAs for Custom Computing Machines, IEEE Computer Society Press, April 19-21, 1995, pp. 155-162.
	<b>**Wada et al., "A Performance Evaluation of Tree-based Coherent Distributed Shared Memory" Proceedings of the Pacific RIM Conference on Communications, Comput and Signal Processing, Victoria, May 19-21 1993, pp. 390-393.</b>
	Weinhardt, Markus et al., "Pipeline Vectorization," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 2, February 2001, pp. 234-248.
	<b>**XLINX, "Logic Cell Array Families: XC4000, XC4000A and XC4000H," product description, pp. 2-7, 2-9, 2-14, 2-15, 8-16, and 9-14.</b>
	<b>** = references cited in earlier statements, but re-cited to correct inadvertent errors in citations.</b>

EXAMINER	/Loren Chauhan/ (03/12/2008)	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /L.C./